PATENT ABSTRACTS OF JAPAN

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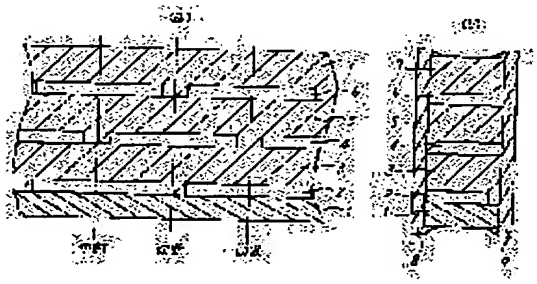
(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD
(72)Inventor : FUJII AKIYUKI
TOMOSAWA ATSUSHI
FUJII SATORU
TAKAYAMA RYOICHI

(54) MANUFACTURE OF LAMINATED THIN-FILM CAPACITOR

(57)Abstract:
PURPOSE: To provide the method of manufacturing a laminated thin-film capacitor, which can miniaturize a chip capacitor and which can make the capacity of the chip capacitor large.
CONSTITUTION: A dielectric thin-film layer 4 in a film thickness of 3μm or lower is formed, by a plasma CVD method, on a substratum substrate 1 on which a metal-electrode thin-film layer 2 has been formed by a vacuum deposition method or a sputtering method. The two layers are laminated alternately, a laminated body is cut in such a way that metal-electrode thin-film layers 2, 4, 6 faced alternately sidewalls every other layer, external electrodes 8, 9 are formed on cut faces, the electrodes are brought into continuity with the metal-electrodes thin-film layers 2, 4, 6 at the inside, and a small and large- capacity laminated thin-film capacitor is manufactured.



LEGAL STATUS

[Date of request for examination]	19.12.1997
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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] Production of a metal-electrode thin film layer which carried out pattern formation by the vacuum deposition method or the sputtering method on the substrate, The laminating of a metal thin film layer and the dielectric thin film layer is carried out by repeating production of the dielectric thin film layer by the plasma-CVD method using the mixed gas of the steam of metallic compounds, and reactant gas by turns. The manufacture approach of the laminating thin film capacitor characterized by forming an external electrode in the cutting plane by the vacuum deposition method, the sputtering method, the galvanizing method, or the spreading burning method after cutting so that said metal-electrode thin film layer which carried out pattern formation may face a side attachment wall alternate for setting further.
[Claim 2] The manufacture approach of the laminating thin film capacitor according to claim 1 characterized by being the perovskite mold oxide with which the ingredient of a dielectric thin film layer uses strontium titanate as a principal component.
[Claim 3] The manufacture approach of the laminating thin film capacitor according to claim 1 characterized by being the compound perovskite mold compound with which the ingredient of a dielectric thin film layer uses Pb (Mg 1/3, Nb 2/3) O3 and lead titanate as a principal component.
[Claim 4] The manufacture approach of the laminating thin film capacitor according to claim 1 characterized by using beta-diketone metal complex or a metal alkoxide as metallic compounds.
[Claim 5] The manufacture approach of the laminating thin film capacitor according to claim 1 characterized by using oxygen, N2O, or H2O as reactant gas.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the manufacture approach of the laminating thin film capacitor used as small and a mass chip capacitor.
[0002]
[Description of the Prior Art] the strontium titanate ($SrTiO_3$) of a perovskite mold crystal structure -- about 110 -- in that of K or more temperature, it is a cubic, and they are paraelectrics. Although a dielectric constant is low compared with the barium titanate ($BaTiO_3$) system of the crystal structure with the same ceramics which used strontium titanate as the principal component, the temperature characteristic has the description that it is good and little dielectric loss is also. Moreover, by adding shifters, such as barium and lead, and shifting the Curie point, in ordinary temperature, the ceramics of the high dielectric constant in paraelectricity is obtained, and it is broadly used as high frequency and a capacitor for high voltages. Moreover, since the compound perovskite structure compound of $Pb(Mg\ 1/3, Nb\ 2/3)\ O_3$-$PbTiO_3$ which is the composite material of $Pb(Mg\ 1/3, Nb\ 2/3)\ O_3$ and lead titanate ($PbTiO_3$) which is one of the typical relaxation mold ferroelectrics has big specific inductive capacity and a good direct-current bias property compared with a barium titanate system ferroelectric, it is applied to the small mass multilayer capacitor etc.
[0003] On the other hand, since it corresponds to the miniaturization of electronic equipment, and high-density-assembly-ization, the miniaturization of a chip capacitor and large capacity-ization are progressing. In order to attain large capacity-ization, there are using dielectric materials with large specific inductive capacity and the approach of making a dielectric layer thin and increasing the number of laminatings. For example, the manufacture approach of a stacked type ceramic condenser is announced by the 61st page from the 57th page (1990) of erection RONIKU ceramic magazine 103 numbers. The laminating approach of a dielectric layer and a metal-electrode layer in manufacture of the stacked type ceramic condenser in this reference is as follows. Slurry preparation of what blends, mixes and dried the powder of dielectric materials, such as $BaTiO_3$, is carried out, and it fabricates on a thin film-like sheet. Internal electrode pastes, such as palladium, are printed on this sheet, and a sheet is accumulated. This actuation is repeated several times, it cuts in that contemptuous glance-magnitude, and it is said that coincidence baking of a ceramic and a metal is performed.
[0004]
[Problem(s) to be Solved by the Invention] However, in order for $BaTiO_3$ of a start raw material to be the powder which is the particle size of about 1 micrometer by the above-mentioned laminating approach, to carry out slurry preparation of this, to fabricate in the shape of a sheet and to calcinate, when it was going to make the dielectric layer thin to 3 micrometers or less, the problem was in the homogeneity and the inter-electrode insulation of thickness, and it was technically difficult. Moreover, burning temperature was as high as about 1200 degrees C, since an electrode material was limited, it was cheap and finding out the manufacture approach of obtaining a multilayer capacitor with a sufficient property at low temperature was called for.
[0005] This invention aims at offering the manufacture approach of the laminating thin film capacitor which enables miniaturization of a chip capacitor, and large capacity-ization with careful attention to said conventional technical problem.
[0006]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, this invention carries out pattern formation of the metal-electrode thin film layer by the vacuum deposition method or the

sputtering method on a substrate. On it as a dielectric thin film layer The compound perovskite mold compound which uses as a principal component the perovskite mold oxide which uses strontium titanate as a principal component, and Pb(Mg 1/3, Nb 2/3) O3 and lead titanate Membranes are formed by the plasma-CVD method using the activity and the CVD reaction of the plasma. What repeated this actuation and carried out the laminating of a metal-electrode thin film layer and the dielectric thin film layer on the substrate is cut in predetermined magnitude, an external electrode is formed in that cutting plane by the vacuum deposition method, the sputtering method, the galvanizing method, or the spreading burning method, and a laminating thin film capacitor is manufactured.

[0007]

[Function] According to this invention, the precise perovskite mold dielectric thin film which uses the good strontium titanate of dielectric characteristics and Pb(Mg 1/3, Nb 2/3) O3-PbTiO3 as a principal component by 3 micrometers or less of thickness is comparatively obtained at low temperature by using a plasma-CVD method for membrane formation of a dielectric thin film layer. Moreover, a too precise and thin metal-electrode thin film layer is obtained by using a vacuum deposition method or the sputtering method for membrane formation of a metal-electrode thin film layer. Therefore, the electrostatic capacity per unit volume becomes large, and the laminating thin film capacitor corresponding to a miniaturization and large-capacity-izing can manufacture at temperature lower than the burning temperature of bulk.

[0008]

[Example]

(Example 1) Drawing 1 shows the schematic diagram of the configuration of the cross section of the laminating thin film capacitor in one example of this invention.

[0009] The substrate substrate with which 1 consists of an alumina in drawing 1 , the metal-electrode thin film layer which 2, 4, and 6 become from metal platinum, the dielectric thin film layer which 3, 5, and 7 become from SrTiO3, and 8 and 9 are external electrodes which consist of silver.

[0010] The manufacture approach of the laminating thin film capacitor which consists of the above-mentioned component is as follows. On the substrate substrate 1, with a vacuum deposition method, as shown in drawing 1 (a), pattern formation of the metal-electrode thin film layer 2 is carried out. Moreover, the dielectric thin film layer 3 is formed by the plasma-CVD method. Furthermore, on it, with a vacuum deposition method, as shown in drawing 1 , in the metal-electrode thin film layer 2, it shifts and pattern formation of the metal-electrode thin film layer 4 is carried out. Furthermore on it, the dielectric thin film layer 5 is formed by the plasma-CVD method. Furthermore, on it, with a vacuum deposition method, the metal-electrode thin film layer 6 is formed by the same pattern as the metal-electrode thin film layer 2, as shown in drawing 1 . Furthermore on it, the dielectric thin film layer 7 is formed by the plasma-CVD method. After repeating this actuation and carrying out the laminating of the predetermined number of layers, as shown in drawing 1 (b), it cuts in predetermined magnitude so that a metal-electrode thin film layer may face a side attachment wall alternate for setting further. The silver external electrodes 8 and 9 are applied to the cutting plane, it can be burned on it, and the internal metal-electrode thin film layers 2 and 46 and the flow of the external electrodes 8 and 9 are taken.

[0011] The membrane formation approach of a dielectric thin film layer is explained below among the above-mentioned manufacture approaches. The schematic diagram of the plasma-CVD equipment used for drawing 2 forming a dielectric thin film layer among the laminating thin film capacitors in one example of this invention is shown.

[0012] As for the substrate substrate with which an electrode and 12 consist in a reaction chamber and 11, and a substrate heating heater and 14 consist [10] of an alumina in a substrate rotary motor and 13, and 15, in drawing 2 , an exhaust air system and 16 are RF generators (13.56MHz) as a component.

[0013] The evaporation containers 17, 18, 19, and 20 into which the raw material went on the other hand are connected to the pipe which carries out opening between the electrodes 11 in a reaction chamber 10 through bulbs 25, 26, 27, and 28. Moreover, the pipe introduced into each of the evaporation containers 17, 18, 19, and 20 It connects with the argon bomb 29 of carrier gas through bulbs 21, 22, 23, and 24, and installation into the reaction chamber 10 of material gas and carrier gas is controlled by closing motion of bulbs 25, 26, 27, and 28. Moreover, the oxygen cylinder 30 is connected to the pipe which carries out opening between the electrodes 11 in a reaction chamber 10. Strontium dipivaloyl methane [Sr (C11H19O2)2] and isopropoxy titanium [Ti (C3H7O)4] were used for the start raw material.

[0014] The membrane formation approach of a dielectric thin film layer is as follows. The substrate substrate 14 which carried out pattern formation of the metal-electrode thin film layer of metal platinum beforehand with the vacuum deposition method was attached in the substrate heating heater 13, and was heated and held at 700 degrees C. Strontium dipivaloyl methane was put into the evaporation container 17, isopropoxy titanium was put into the evaporation container 18, and it heated and held at 235 degrees C and 50 degrees C, respectively. The inside of a reaction chamber 10 was exhausted by the exhaust air system 15, and the substrate substrate 14 was rotated at the rate of per minute 120 rotation the whole substrate heating heater 13 with the substrate rotary motor 12. Bulbs 17, 18, 25, and 26 are opened. With carrier gas (they are flow rate 25SCCM and 5SCCM to carburetors 17 and 18, respectively) The steam of strontium dipivaloyl methane and isopropoxy titanium It introduces in a reaction chamber 10 with the oxygen (flow rate 10SCCM) which is reactant gas. In the plasma (power 1.4 W/cm2), it reacted under reduced pressure (0.02Torr) for 50 minutes, and the thin film of SrTiO3 which is a dielectric thin film layer was formed on the substrate substrate 14 which carried out pattern formation of the metal-electrode thin film layer. This was taken out after [cooling] picking, pattern formation of the metal-electrode thin film layer was again carried out on the dielectric thin film layer with the vacuum deposition method, and the dielectric thin film layer was formed by the same approach as the above on it. The rest repeated this actuation and accumulated a metal-electrode thin film layer and ten layers of dielectric thin film layers at a time. This was cut in predetermined magnitude the whole substrate so that a metal-electrode thin film layer might face a side attachment wall alternate for setting further, as shown in drawing 1 , silver was applied and baked on the cutting plane, and the external electrode was formed.

[0015] Moreover, the sample which formed metal platinum on the alumina substrate and formed only one layer of thin films of SrTiO3 by the completely same approach as the above on it to analysis of a dielectric thin film layer was produced.

[0016] The thickness of the dielectric thin film layer of the obtained laminating thin film capacitor was 2.2 micrometers of hits much more, and the thickness of a metal-electrode thin film layer was 0.06 micrometers of hits much more. The electrical property was measured between the electrode 8 of this laminating thin film capacitor, and 9. When dielectric characteristics were measured at 1kHz, 1V, and a room temperature with the LCR meter, specific inductive capacity was 190 and dielectric loss was 0.06. Insulation resistance was more than 109ohm and cm, and direct-current breakdown voltage was 0.7 kV/cm. Moreover, when analysis by the X diffraction was performed by the sample which formed metal platinum on the alumina substrate and formed only one layer of thin films of SrTiO3 on it, it was the perovskite mold crystal structure.

[0017] In addition, in the above-mentioned example, although strontium dipivaloyl methane and isopropoxy titanium were used as a raw material of Sr and Ti, in the manufacture approach of this example, without being limited to this raw material, the thin film of SrTiO3 of the perovskite mold crystal structure could be obtained, and it checked that equivalent dielectric characteristics were obtained. Moreover, when N2O and H2O were used as reactant gas, it checked that dielectric characteristics equivalent to the case where oxygen is used were obtained.

[0018] The same result was obtained when barium, lead, a bismuth, calcium, and magnesium were added as an additive.

(Example 2) Drawing 3 shows the schematic diagram of the configuration of the cross section of the laminating thin film capacitor in the example 2 of this invention.

[0019] The substrate substrate with which 31 consists of an alumina as a component in drawing 3 , the metal-electrode thin film layer which 32, 34, and 36 become from metal platinum, the dielectric thin film layer which 33, 35, and 37 become from Pb(Mg 1/3, Nb 2/3) O3-PbTiO3, and 38 and 39 are external electrodes which consist of silver.

[0020] The manufacture approach of this laminating thin film capacitor is as follows. On the substrate substrate 31, with a vacuum deposition method, as shown in drawing 3 (a), pattern formation of the metal-electrode thin film layer 32 is carried out. The dielectric thin film layer 33 is formed by the plasma-CVD method on it. On it, with a vacuum deposition method, as furthermore shown in drawing 3 (a), in the metal-electrode thin film layer 32, it shifts and pattern formation of the metal-electrode thin film layer 34 is carried out. Furthermore, the dielectric thin film layer 35 is formed by the plasma-CVD method on it. On it, with a vacuum deposition method, the metal-electrode thin film layer 36 is formed by the same pattern as the metal-electrode thin film layer 32, as furthermore shown in drawing 3 (a). Furthermore, the dielectric thin film layer 37 is formed by the

plasma-CVD method on it. After repeating this actuation and carrying out the laminating of the predetermined number of layers, as shown in drawing 3 (b), it cuts in predetermined magnitude so that the metal-electrode thin film layers 32, 34, and 36 may face a side attachment wall alternate for setting further. The silver external electrodes 38 and 39 are applied to the cutting plane, it can be burned on it, and the internal metal-electrode thin film layers 32, 34, and 36 and the flow of the external electrodes 38 and 39 are taken.

[0021] The membrane formation approach of the dielectric thin film layers 33, 35, and 37 is explained below among the above-mentioned manufacture approaches. Lead dipivaloyl methane [Pb (C11H19O2)2], isopropoxy titanium [Ti (C3H7O)4], magnesium acetylacetonato [Mg(C5H7O2) 2andH2O], and pentaethoxy niobium [Nb (OC2H5)5] were used for the start raw material.

[0022] This thing also attached in the substrate heating heater 13 the substrate substrate 14 which carried out pattern formation of the metal-electrode thin film layer of metal platinum beforehand with the vacuum deposition method, as shown in drawing 2 , and it heated and held it at 700 degrees C. the evaporation container 17 -- lead dipivaloyl methane -- in the evaporation container 18, magnesium acetylacetonato was put into the evaporation container 19, pentaethoxy niobium was put into the evaporation container 20, and isopropoxy titanium was heated at 145 degrees C, 50 degrees C, 195 degrees C, and 60 degrees C, and was held, respectively. Exhausting the inside of a reaction chamber 10 by the exhaust air system 15, the substrate heating heater rotated at the rate of per minute 120 rotation with the substrate rotary motor 12. Bulbs 21, 22, 23, 24, 25, 26, 27, and 28 are opened. With carrier gas (they are flow rate 35SCCM, 15SCCM, 10SCCM, and 8SCCM to carburetors 17, 18, 19, and 20, respectively) Lead dipivaloyl methane, isopropoxy titanium, magnesium acetylacetonato, The steam of pentaethoxy niobium is introduced in a reaction chamber 10 with the oxygen (flow rate 30SCCM) which is reactant gas. In the plasma (power 1.4 W/cm2), it reacted under reduced pressure (0.03Torr) for 50 minutes, and the thin film of Pb(Mg 1/3, Nb 2/3) O3-PbTiO3 which is a dielectric thin film layer was formed on the substrate substrate 14 which carried out pattern formation of the metal-electrode thin film layer. This was taken out after [cooling] picking, pattern formation of the metal-electrode thin film layer was again carried out on the dielectric thin film layer with the vacuum deposition method, and the dielectric thin film layer was formed by the same approach as the above on it. The rest repeated this actuation and accumulated a metal-electrode thin film layer and ten layers of dielectric thin film layers at a time. This was cut in predetermined magnitude the whole substrate so that a metal-electrode thin film layer might face a side attachment wall alternate for setting further, as shown in drawing 3 , silver was applied and baked on the cutting plane, and the external electrode was formed.

[0023] Moreover, the sample which formed metal platinum on the alumina substrate and formed only one layer of thin films of SrTiO3 by the completely same approach as the above on it to analysis of a dielectric thin film layer was produced.

[0024] The thickness of the dielectric thin film layer of the obtained laminating thin film capacitor was 2.2 micrometers of hits much more, and the thickness of a metal-electrode thin film layer was 0.06 micrometers of hits much more. The electrical property was measured between the electrode 8 of this laminating thin film capacitor, and 9. When dielectric characteristics were measured at 1kHz, 1V, and a room temperature with the LCR meter, specific inductive capacity was 190 and dielectric loss was 0.06. Insulation resistance was more than 109ohm and cm, and direct-current breakdown voltage was 0.7 kV/cm. Moreover, when analysis by the X diffraction was performed by the sample which formed metal platinum on the alumina substrate and formed only one layer of thin films of Pb(Mg 1/3, Nb 2/3) O3-PbTiO3 on it, it was the perovskite mold crystal structure. The film presentation analyzed by the X-ray microanalyser was Pb{(Mg1/3Nb 2/3) 0.7Ti0.3} O3.

[0025] In addition, in the above-mentioned example, although lead dipivaloyl methane, isopropoxy titanium, magnesium acetylacetonato, and pentaethoxy niobium were used as a raw material of Pb, Ti, Mg, and Nb, in the manufacture approach of this example, without being limited to this raw material, Pb(Mg 1/3, Nb 2/3) O3-PbTiO3 thin film of the perovskite mold crystal structure could be obtained, and it checked that equivalent dielectric characteristics were obtained. Moreover, when N2O and H2O were used as reactant gas, it checked that dielectric characteristics equivalent to the case where oxygen is used were obtained.

[0026] The same result was obtained when barium, strontium, a bismuth, calcium, nickel, zinc, cobalt, iron, a tantalum, and a tungsten were added as an additive.

[0027] In examples 1 and 2, when metals other than platinum, for example, palladium, palladium / silver alloy, nickel, copper, etc. were used for the metal-electrode thin film layer with vacuum evaporation technique, or

even when the sputtering method was used for the membrane formation approach, manufacture of a laminating thin film capacitor with an equivalent property was possible. Manufacture of the laminating thin film capacitor which similarly has an equivalent property in it when metals other than silver were used, or even when a vacuum deposition method, the sputtering method, or the galvanizing method is used for formation of an external electrode in addition to the spreading burning method was possible.

[0028] Moreover, in examples 1 and 2, although the plasma-CVD equipment which forms a dielectric thin film layer, and the vacuum evaporation system and sputtering system which form a metal-electrode thin film layer were another, when conveying the substrate and forming membranes continuously using the connected equipment, without breaking a vacuum, it was able to manufacture still more easily.

[0029]

[Effect of the Invention] When this invention uses a plasma-CVD method for membrane formation of a dielectric thin film layer, the precise thin film of good SrTiO3 of dielectric characteristics or Pb(Mg 1/3, Nb 2/3) O3-PbTiO3 is comparatively obtained at low temperature on a metal-electrode thin film layer, so that more clearly than explanation of the above example. Moreover, a too precise and thin metal-electrode thin film layer is obtained by using a vacuum deposition method or the sputtering method for membrane formation of a metal-electrode thin film layer. Therefore, since it can do more thinly than the approach of accumulating and calcinating the thing of the shape of a slurry in the conventional stacked type ceramic condenser, also by the same chip thickness, the number of laminatings increases, electrostatic capacity becomes large, and it can respond to a miniaturization and large capacity-ization.

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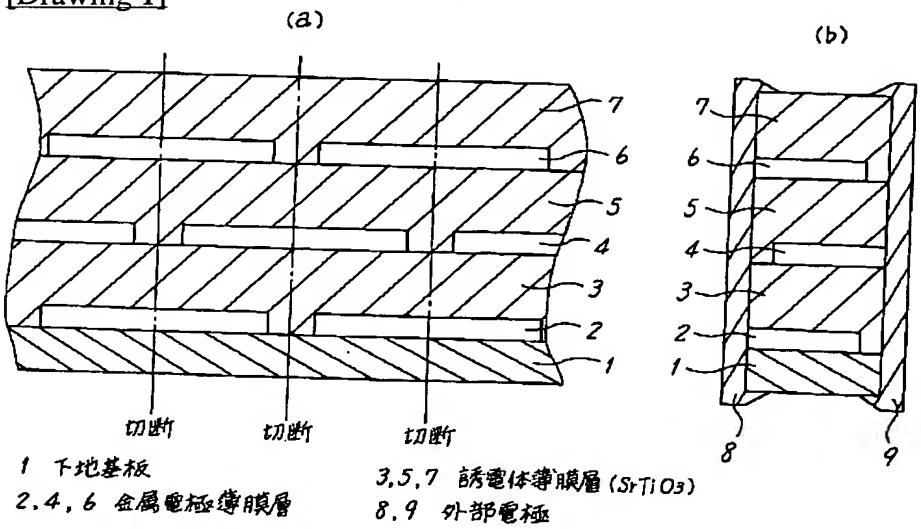
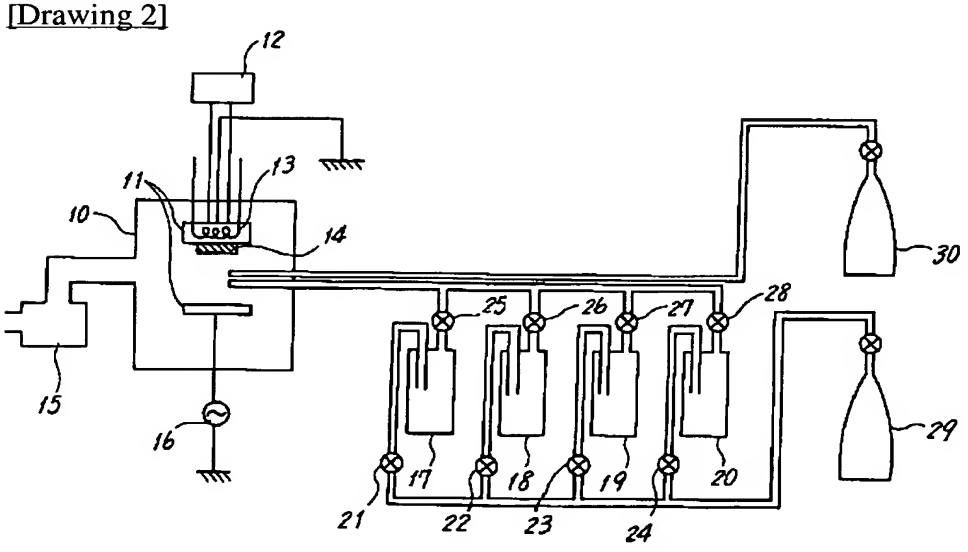
DRAWINGS

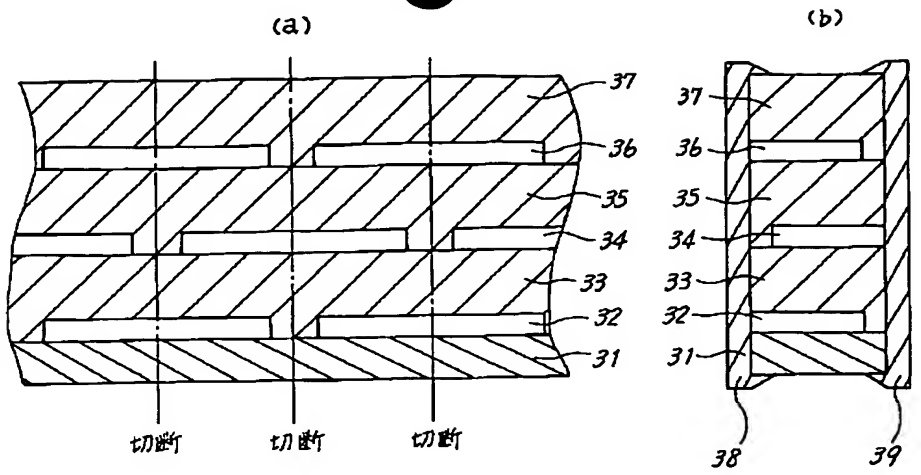
[Drawing 1]



[Drawing 2]



[Drawing 3]



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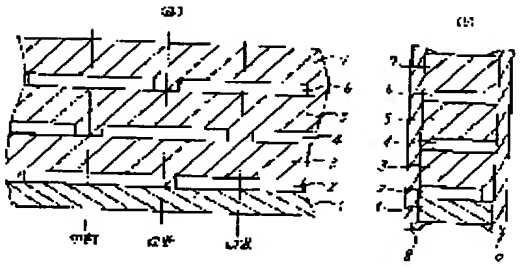
CONSTITUTION: A dielectric thin-film layer 4 in a film thickness of 3μm or lower is formed, by a plasma CVD method, on a substratum substrate 1 on which a metal-electrode thin-film layer 2 has been formed by a vacuum deposition method or a sputtering method. The two layers are laminated alternately, a laminated body is cut in such a way that metal-electrode thin-film layers 2, 4, 6 faced alternately sidewalls every other layer, external electrodes 8, 9 are formed on cut faces, the electrodes are brought into continuity with the metal-electrodes thin-film layers 2, 4, 6 at the inside, and a small and large- capacity laminated thin-film capacitor is manufactured.



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	4/10					
	4/12	３６４				
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			9174－5E		4/10	

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(71)出願人　000005821
松下電器産業株式会社
大阪府門真市大字門真1006番地

(72)発明者　藤井　映志
大阪府門真市大字門真1006番地　松下電器産業株式会社内

(72)発明者　友澤　淳
大阪府門真市大字門真1006番地　松下電器産業株式会社内

(72)発明者　藤井　覚
大阪府門真市大字門真1006番地　松下電器産業株式会社内

(74)代理人　弁理士　森本　義弘

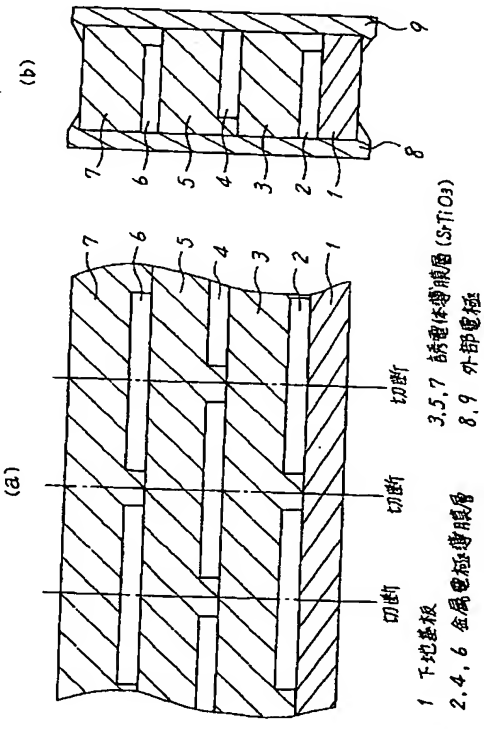
最終頁に続く

(54)【発明の名称】　積層薄膜コンデンサの製造方法

(57)【要約】

【目的】　本発明は、チップコンデンサの小型化、大容量化を可能とする積層薄膜コンデンサの製造方法を提供することを目的とする。

【構成】　真空蒸着法またはスパッタリング法により、金属電極薄膜層２をパターン形成した下地基板１上に、プラズマＣＶＤ法により誘電体薄膜層３を３μｍ以下の膜厚で成膜する。この２つの層を交互に積層した後、金属電極薄膜層２、４、６が一層おきに互い違いの側壁に面する様に切断し、その切断面に外部電極８、９を形成し、内部の金属電極薄膜層２、４、６と導通をとり、小型、大容量の積層薄膜コンデンサを作製する。



【特許請求の範囲】
【請求項１】　基板上に、真空蒸着法またはスパッタリング法によりパターン形成した金属電極薄膜層の作製と、金属化合物の蒸気と反応ガスとの混合ガスを用いたプラズマＣＶＤ法による誘電体薄膜層の作製を交互に繰り返すことにより金属薄膜層と誘電体薄膜層を積層し、前記パターン形成した金属電極薄膜層が一層おきに互い違いの側壁に面するように切断した後、その切断面に外部電極を真空蒸着法またはスパッタリング法またはめっき法または塗布焼付け法により形成することを特徴とする積層薄膜コンデンサの製造方法。
【請求項２】　誘電体薄膜層の材料がチタン酸ストロンチウムを主成分とするペロブスカイト型酸化物であることを特徴とする請求項１記載の積層薄膜コンデンサの製造方法。
【請求項３】　誘電体薄膜層の材料がＰｂ（$Mg_{1/3}$, $Nb_{2/3}$）O_3とチタン酸鉛を主成分とする複合ペロブスカイト型化合物であることを特徴とする請求項１記載の積層薄膜コンデンサの製造方法。
【請求項４】　金属化合物としてβ－ジケトン金属錯体または金属アルコキシドを用いることを特徴とする請求項１記載の積層薄膜コンデンサの製造方法。
【請求項５】　反応ガスとして酸素またはN_2OまたはH_2Oを用いることを特徴とする請求項１記載の積層薄膜コンデンサの製造方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、小型、大容量チップコンデンサとして用いられる、積層薄膜コンデンサの製造方法に関する。
【０００２】
【従来の技術】ペロブスカイト型結晶構造のチタン酸ストロンチウム（$SrTiO_3$）は、約１１０Ｋ以上の温度のにおいては立方晶であり常誘電体である。チタン酸ストロンチウムを主成分としたセラミックスは、同じ結晶構造のチタン酸バリウム（$BaTiO_3$）系に比べて誘電率は低いが、温度特性がよく誘電損失も少ないといった特徴を有する。また、バリウムや鉛などのシフタを加えてキュリー点をシフトさせることにより、常温において常誘電性で高誘電率のセラミックスが得られ、高周波・高電圧用コンデンサとして幅広く利用されている。また、代表的な緩和型強誘電体の一つである$Pb(Mg_{1/3}, Nb_{2/3})O_3$とチタン酸鉛（$PbTiO_3$）の複合材料である$Pb(Mg_{1/3}, Nb_{2/3})O_3$－$PbTiO_3$の複合ペロブスカイト構造化合物は、チタン酸バリウム系強誘電体に比べて、大きな比誘電率と良好な直流バイアス特性を有するため、小型大容量積層コンデンサなどに応用されている。
【０００３】一方、電子機器の小型化、高密度実装化に対応するため、チップコンデンサの小型化、大容量化が進んでいる。大容量化を達成するには、比誘電率の大きい誘電体材料を用いることや、誘電体層を薄くして積層数を増加する方法がある。たとえば、エレクトロニク・セラミック誌１０３号（１９９０年）第５７頁から第６１頁に積層セラミックコンデンサの製造方法が発表されている。この文献での積層セラミックコンデンサの製造における誘電体層と金属電極層の積層方法は以下の通りである。$BaTiO_3$などの誘電体材料の粉末を配合、混合し、かつ乾燥させたものをスラリ調合して薄膜状のシートに成形する。このシートにパラジウムなどの内部電極ペーストを印刷し、シートを積み重ねる。この操作を数回繰り返し、その後目的の大きさに切断し、セラミックと金属の同時焼成を行うといったものである。
【０００４】
【発明が解決しようとする課題】しかしながら、上記積層方法では、出発原料の$BaTiO_3$が粒径１μｍ程度の粉末であり、これをスラリ調合し、シート状に成形して焼成するため、誘電体層を３μｍ以下に薄くしようとすると、膜厚の均一性や電極間の絶縁性に問題があり、技術的に困難であった。また焼成温度が約１２００℃と高く、電極材料が限定されるため、安価で特性の良い積層コンデンサを低温で得る製造方法を見出すことが求められていた。
【０００５】本発明は前記従来の課題に留意し、チップコンデンサの小型化、大容量化を可能とする積層薄膜コンデンサの製造方法を提供することを目的とする。
【０００６】
【課題を解決するための手段】上記課題を解決するために本発明は、基板上に金属電極薄膜層を真空蒸着法またはスパッタリング法によってパターン形成し、その上に誘電体薄膜層として、チタン酸ストロンチウムを主成分とするペロブスカイト型酸化物や$Pb(Mg_{1/3}, Nb_{2/3})O_3$とチタン酸鉛を主成分とする複合ペロブスカイト型化合物を、プラズマの活性とＣＶＤ反応を利用したプラズマＣＶＤ法によって成膜し、この操作を繰り返して基板上に金属電極薄膜層と誘電体薄膜層を積層したものを所定の大きさに切断し、その切断面に外部電極を真空蒸着法またはスパッタリング法またはめっき法または塗布焼付け法によって形成して積層薄膜コンデンサを製造するものである。
【０００７】
【作用】本発明によれば、誘電体薄膜層の成膜にプラズマＣＶＤ法を用いることにより、膜厚３μｍ以下で、誘電特性の良好なチタン酸ストロンチウムや$Pb(Mg_{1/3}, Nb_{2/3})O_3$－$PbTiO_3$を主成分とする緻密なペロブスカイト型誘電体薄膜が比較的低温で得られる。また、金属電極薄膜層の成膜に真空蒸着法またはスパッタリング法を用いることにより、やはり緻密で薄い金属電極薄膜層が得られる。よって、単位体積あたりの静電容量が大きくなり、小型化、大容量化に対応した積層薄膜

コンデンサが、バルクの焼成温度よりも低い温度で製造できることとなる。

【０００８】

【実施例】

（実施例１）図１は、本発明の一実施例における積層薄膜コンデンサの断面の構成の概略図を示すものである。

【０００９】図１において１はアルミナからなる下地基板、２、４、６は金属白金からなる金属電極薄膜層、３、５、７は$SrTiO_3$からなる誘電体薄膜層、８、９は銀からなる外部電極である。

【００１０】上記構成要素よりなる積層薄膜コンデンサの製造方法は以下の通りである。下地基板１上に、金属電極薄膜層２を真空蒸着法によって図１（ａ）に示すようにパターン形成する。その上に、誘電体薄膜層３をプラズマＣＶＤ法により形成する。さらにその上に、金属電極薄膜層４を真空蒸着法によって、図１に示すように金属電極薄膜層２とはずらしてパターン形成する。さらにその上に、誘電体薄膜層５をプラズマＣＶＤ法により形成する。さらにその上に、金属電極薄膜層６を真空蒸着法によって、図１に示すように金属電極薄膜層２と同じパターンで形成する。さらにその上に、誘電体薄膜層７をプラズマＣＶＤ法により形成する。この操作を繰り返して、所定の層数を積層した後、図１（ｂ）に示すように、金属電極薄膜層が一層おきに互い違いの側壁に面するように所定の大きさに切断する。その切断面に、銀の外部電極８、９を塗布し、焼き付けて内部の金属電極薄膜層２、４６と外部電極８、９の導通をとる。

【００１１】上記の製造方法のうち、誘電体薄膜層の成膜方法について以下に説明する。図２は、本発明の一実施例における積層薄膜コンデンサのうち、誘電体薄膜層を成膜するのに用いるプラズマＣＶＤ装置の概略図を示すものである。

【００１２】図２において構成要素として１０は反応チャンバー、１１は電極、１２は基板回転モーター、１３は基板加熱ヒーター、１４はアルミナからなる下地基板、１５は排気系、１６は高周波電源（１３．５６MHz）である。

【００１３】一方原料の入った気化容器１７、１８、１９、２０はバルブ２５、２６、２７、２８を介して反応チャンバー１０における電極１１の間に開口するパイプに接続され、また、気化容器１７、１８、１９、２０のそれぞれに導入されたパイプは、バルブ２１、２２、２３、２４を介してキャリアガスのアルゴンボンベ２９に接続されており、バルブ２５、２６、２７、２８の開閉により原料ガスとキャリアガスの反応チャンバー１０内への導入が制御される。また、酸素ボンベ３０は、反応チャンバー１０における電極１１の間に開口するパイプに接続されている。出発原料にはストロンチウムジピバロイルメタン〔$Sr(C_{11}H_{19}O_2)_2$〕、およびイソプロポキシチタン〔$Ti(C_3H_7O)_4$〕を用いた。

【００１４】誘電体薄膜層の成膜方法は以下の通りである。真空蒸着法により予め金属白金の金属電極薄膜層をパターン形成した下地基板１４を、基板加熱ヒーター１３に取り付け、７００℃に加熱し保持した。気化容器１７にストロンチウムジピバロイルメタンを、気化容器１８にイソプロポキシチタンを入れ、それぞれ２３５℃、５０℃に加熱し保持した。反応チャンバー１０内を排気系１５によって排気し、基板回転モーター１２によって、基板加熱ヒーター１３ごと下地基板１４を毎分１２０回転の速度で回転した。バルブ１７、１８、２５、２６を開き、キャリアガス（気化器１７、１８にそれぞれ流量２５SCCM、５SCCM）により、ストロンチウムジピバロイルメタン、イソプロポキシチタンの蒸気を、反応ガスである酸素（流量１０SCCM）とともに反応チャンバー１０内に導入し、プラズマ中（電力１．４W／cm^2）で５０分間減圧下（０．０２Torr）で反応を行い、誘電体薄膜層である$SrTiO_3$の薄膜を、金属電極薄膜層をパターン形成した下地基板１４の上に成膜した。これを冷却後取り出して、再び真空蒸着法で金属電極薄膜層を誘電体薄膜層上にパターン形成し、その上に上記と同じ方法で誘電体薄膜層を成膜した。後はこの操作を繰り返して、金属電極薄膜層と誘電体薄膜層を１０層ずつ積み重ねた。これを、図１に示したように、金属電極薄膜層が一層おきに互い違いの側壁に面するように基板ごと所定の大きさに切断し、切断面に銀を塗布して焼付け、外部電極を形成した。

【００１５】また誘電体薄膜層の分析用に、アルミナ基板上に金属白金を成膜し、その上に$SrTiO_3$の薄膜を、上記と全く同じ方法で一層だけ成膜した試料を作製した。

【００１６】得られた積層薄膜コンデンサの誘電体薄膜層の膜厚は一層あたり２．２μmで、金属電極薄膜層の膜厚は一層あたり０．０６μmであった。この積層薄膜コンデンサの電極８、９間で電気特性を測定した。誘電特性は、ＬＣＲメーターにより１kHz、１V、室温で測定すると、比誘電率が１９０、誘電損失が０．０６であった。絶縁抵抗は$10^9\Omega$・cm以上で、直流破壊電圧は０．７kV／cmであった。また、アルミナ基板上に金属白金を成膜し、その上に$SrTiO_3$の薄膜を一層だけ成膜した試料で、Ｘ線回折による分析を行ったところ、ペロブスカイト型結晶構造であった。

【００１７】なお、上記実施例では、ＳｒとＴｉの原料としてストロンチウムジピバロイルメタン、イソプロポキシチタンを用いたが、本実施例の製造方法ではこの原料に限定されることなく、ペロブスカイト型結晶構造の$SrTiO_3$の薄膜を得ることができ、同等の誘電特性が得られることを確認した。また、反応ガスとしてN_2OやH_2Oを用いた場合においても酸素を用いた場合と同等の誘電特性が得られることを確認した。

【００１８】添加物としてバリウム、鉛、ビスマス、カ

ルシウム、マグネシウムを加えた場合においても同様の結果が得られた。

（実施例２）図３は、本発明の実施例２における積層薄膜コンデンサの断面の構成の概略図を示すものである。

【００１９】図３において構成要素として３１はアルミナからなる下地基板、３２、３４、３６は金属白金からなる金属電極薄膜層、３３、３５、３７はＰｂ（Ｍｇ1/3，Ｎｂ2/3）Ｏ3－ＰｂＴｉＯ3からなる誘電体薄膜層、３８、３９は銀からなる外部電極である。

【００２０】この積層薄膜コンデンサの製造方法は以下の通りである。下地基板３１上に金属電極薄膜層３２を真空蒸着法によって、図３（ａ）に示すようにパターン形成する。その上に誘電体薄膜層３３をプラズマＣＶＤ法により形成する。さらにその上に金属電極薄膜層３４を真空蒸着法によって、図３（ａ）に示すように金属電極薄膜層３２とはずらしてパターン形成する。さらにその上に誘電体薄膜層３５をプラズマＣＶＤ法により形成する。さらにその上に金属電極薄膜層３６を真空蒸着法によって、図３（ａ）に示すように金属電極薄膜層３２と同じパターンで形成する。さらにその上に誘電体薄膜層３７をプラズマＣＶＤ法により形成する。この操作を繰り返して所定の層数を積層した後、図３（ｂ）に示すように、金属電極薄膜層３２、３４、３６が一層おきに互い違いの側壁に面するように所定の大きさに切断する。その切断面に銀の外部電極３８、３９を塗布し、焼き付けて内部の金属電極薄膜層３２、３４、３６と外部電極３８、３９の導通をとる。

【００２１】上記の製造方法のうち、誘電体薄膜層３３、３５、３７の成膜方法について以下に説明する。出発原料には鉛ジピバロイルメタン〔Ｐｂ（$C_{11}H_{19}O_2$）2〕、イソプロポキシチタン〔Ｔｉ（C_3H_7O）4〕、マグネシウムアセチルアセトナート〔Ｍｇ（$C_5H_7O_2$）2・H_2O〕、ペンタエトキシニオブ〔Ｎｂ（OC_2H_5）5〕を用いた。

【００２２】このものも図２に示すように真空蒸着法により予め金属白金の金属電極薄膜層をパターン形成した下地基板１４を、基板加熱ヒーター１３に取り付け、７００℃に加熱し保持した。気化容器１７に鉛ジピバロイルメタンを、気化容器１８にイソプロポキシチタンを、気化容器１９にマグネシウムアセチルアセトナートを、気化容器２０にペンタエトキシニオブを入れ、それぞれ１４５℃、５０℃、１９５℃、６０℃に加熱し保持した。反応チャンバー１０内を排気系１５によって排気し、基板回転モーター１２によって、基板加熱ヒーターは毎分１２０回転の速度で回転した。バルブ２１、２２、２３、２４、２５、２６、２７、２８を開き、キャリアガス（気化器１７、１８、１９、２０にそれぞれ流量３５SCCM、１５SCCM、１０SCCM、８SCCM）により、鉛ジピバロイルメタン、イソプロポキシチタン、マグネシウムアセチルアセトナート、ペンタエトキシニオブの蒸気を、反応ガスである酸素（流量３０SCCM）とともに反応チャンバー１０内に導入し、プラズマ中（電力１．４Ｗ／cm_2）で５０分間減圧下（０．０３Torr）で反応を行い、誘電体薄膜層であるＰｂ（Ｍｇ1/3，Ｎｂ2/3）Ｏ3－ＰｂＴｉＯ3の薄膜を、金属電極薄膜層をパターン形成した下地基板１４の上に成膜した。これを冷却後取り出して、再び真空蒸着法で金属電極薄膜層を誘電体薄膜層上にパターン形成し、その上に上記と同じ方法で誘電体薄膜層を成膜した。後はこの操作を繰り返して、金属電極薄膜層と誘電体薄膜層を１０層ずつ積み重ねた。これを、図３に示したように、金属電極薄膜層が一層おきに互い違いの側壁に面するように基板ごと所定の大きさに切断し、切断面に銀を塗布して焼付け、外部電極を形成した。

【００２３】また誘電体薄膜層の分析用に、アルミナ基板上に金属白金を成膜し、その上にＳｒＴｉＯ3の薄膜を、上記と全く同じ方法で一層だけ成膜した試料を作製した。

【００２４】得られた積層薄膜コンデンサの誘電体薄膜層の膜厚は一層あたり２．２μｍで、金属電極薄膜層の膜厚は一層あたり０．０６μｍであった。この積層薄膜コンデンサの電極８、９間で電気特性を測定した。誘電特性は、ＬＣＲメーターにより１ｋＨｚ、１Ｖ、室温で測定すると、比誘電率が１９０、誘電損失が０．０６であった。絶縁抵抗は10^9Ω・ｃｍ以上で、直流破壊電圧は０．７ｋＶ／ｃｍであった。また、アルミナ基板上に金属白金を成膜し、その上にＰｂ（Ｍｇ1/3，Ｎｂ2/3）Ｏ3－ＰｂＴｉＯ3の薄膜を一層だけ成膜した試料で、Ｘ線回折による分析を行ったところ、ペロブスカイト型結晶構造であった。Ｘ線マイクロアナライザーにより分析した膜組成はＰｂ｛（Ｍｇ1/3Ｎｂ2/3）0.7Ｔｉ0.3｝Ｏ3であった。

【００２５】なお、上記実施例では、Ｐｂ、Ｔｉ、Ｍｇ、Ｎｂの原料として鉛ジピバロイルメタン、イソプロポキシチタン、マグネシウムアセチルアセトナート、ペンタエトキシニオブを用いたが、本実施例の製造方法ではこの原料に限定されることなく、ペロブスカイト型結晶構造のＰｂ（Ｍｇ1/3，Ｎｂ2/3）Ｏ3－ＰｂＴｉＯ3薄膜を得ることができ、同等の誘電特性が得られることを確認した。また、反応ガスとしてN_2OやH_2Oを用いた場合においても酸素を用いた場合と同等の誘電特性が得られることを確認した。

【００２６】添加物としてバリウム、ストロンチウム、ビスマス、カルシウム、ニッケル、亜鉛、コバルト、鉄、タンタル、タングステンを加えた場合においても同様の結果が得られた。

【００２７】実施例１および２において、金属電極薄膜層に、真空蒸着法により白金以外の金属、たとえばパラジウム、パラジウム／銀合金、ニッケル、銅等を用いた場合や、成膜方法にスパッタリング法を用いた場合で

も、同等の特性を持つ積層薄膜コンデンサの製造が可能であった。同様に、外部電極の形成に、銀以外の金属を用いた場合や、塗布焼付け法以外に真空蒸着法またはスパッタリング法またはめっき法を用いた場合でも、同等の特性を持つ積層薄膜コンデンサの製造が可能であった。

【００２８】また、実施例１および２においては、誘電体薄膜層を成膜するプラズマＣＶＤ装置と、金属電極薄膜層を成膜する真空蒸着装置やスパッタリング装置が別になっていたが、連結した装置を用いて、真空を破らずに基板を搬送して連続して成膜すれば、さらに容易に製造することができた。

【００２９】

【発明の効果】以上の実施例の説明より明らかなように、本発明は誘電体薄膜層の成膜にプラズマＣＶＤ法を用いることによって、金属電極薄膜層上に、誘電特性の良好な$SrTiO_3$または$Pb(Mg_{1/3}Nb_{2/3})O_3$－$PbTiO_3$の緻密な薄膜が、比較的低温で得られる。また、金属電極薄膜層の成膜に真空蒸着法またはスパッタリング法を用いることによって、やはり緻密で薄い金属電極薄膜層が得られる。したがって、従来の積層セラミックコンデンサでのスラリ状のものを積み重ねて焼成する方法よりも薄くできるため、同じチップ厚みでも積層数が増え、静電容量が大きくなり、小型化、大容量化に対応できる。

【図面の簡単な説明】

【図１】本発明の一実施例の積層薄膜コンデンサの断面の概略図

【図２】本発明の一実施例の積層薄膜コンデンサの誘電体薄膜層を成膜するために使用するプラズマＭＯＣＶＤ装置の概略図

【図３】本発明の他の実施例の積層薄膜コンデンサの断面の概略図

【符号の説明】

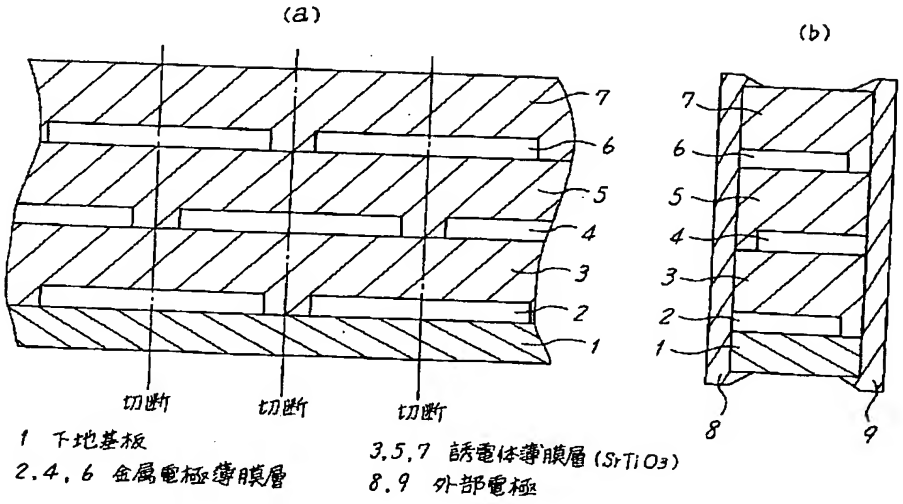
１　下地基板

２、４、６　金属電極薄膜層

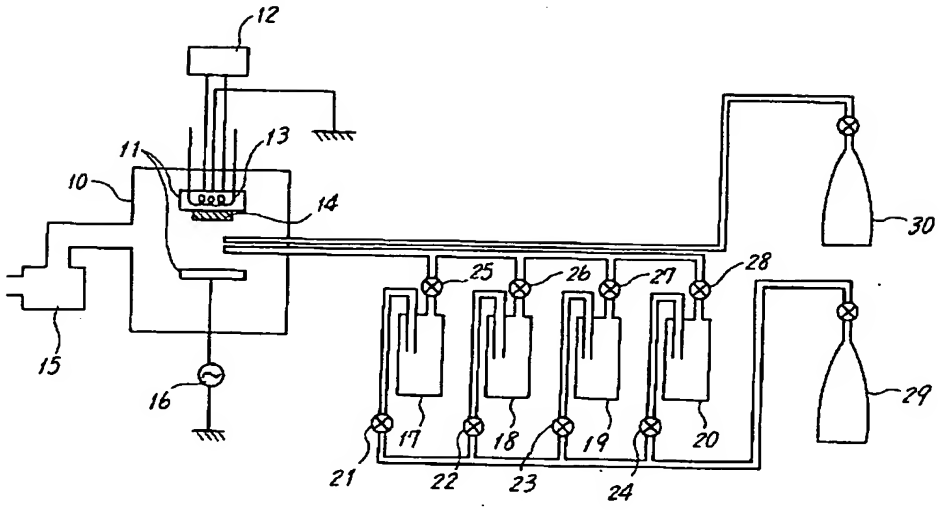
３、５、７　$SrTiO_3$誘電体薄膜層

８、９　外部電極

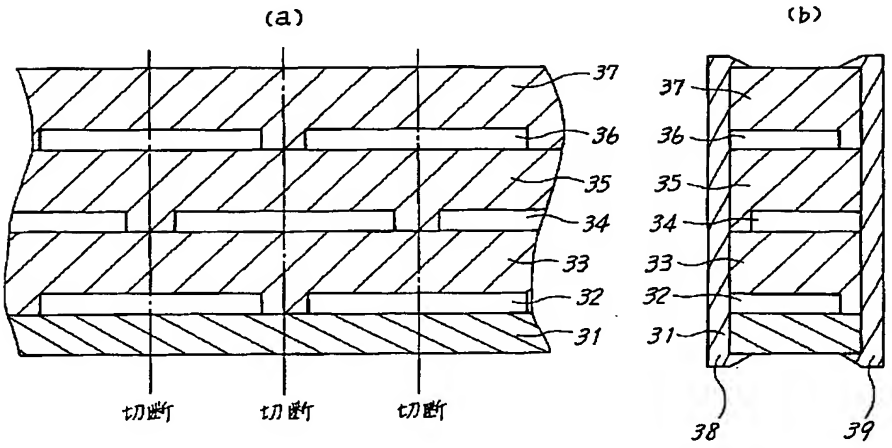
【図１】



【図2】



【図3】



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(72) 発明者　高山　良一
大阪府門真市大字門真1006番地　松下電器
産業株式会社内